CLAIMS

What is claimed is:

1. A method of manufacturing, comprising:

forming a symmetric transistor and an asymmetric transistor on a substrate, the symmetric transistor having a first gate on the substrate, a first source/drain region and second source/drain region in the substrate, the asymmetric transistor having a second gate on the substrate, a first source region and a first drain region in the substrate;

forming a first mask on the substrate with a first opening to enable implantation of first and second halo regions proximate the first and second source/drain regions of the symmetric transistor;

forming the first and second halo regions of a first dosage beneath the first gate by implanting off-axis through the first opening at a first twist angle and then a second and substantially opposite twist angle;

removing the first mask;

forming a second mask on the substrate with a second opening to enable implantation formation of a third halo region proximate the first source region of the second asymmetric transistor but prevent formation of a halo region proximate the first drain region; and

forming the third halo region of a second dosage greater than the first dosage by implanting off-axis through the second opening.

2. The method of claim 1, wherein the second dosage is about twice the first dosage.

3. The method of claim 1, comprising forming the symmetric and asymmetric transistors on a shared active region.

4. The method of claim 1, wherein the symmetric transistor is formed adjacent to the asymmetric transistor.

5. The method of claim 1, wherein the symmetric transistor is not formed adjacent to the asymmetric transistor.

6. The method of claim 1, wherein the third halo region is formed by implanting at a RIGHT twist angle or a LEFT twist angle relative to the second gate.

7. The method of claim 1, wherein the second opening extends to either side of the second gate.

8. The method of claim 7, wherein the second opening extends different distances from opposite sides of the second gate.

9. A method of manufacturing, comprising:

forming a symmetric transistor having a first gate on the substrate, a first source/drain region and second source/drain region in a substrate and an asymmetric transistor having a second gate on the substrate, a first source region and a first drain region in the substrate;

forming a first mask on the substrate, the first mask having a first opening exposing a first portion of the first source/drain region proximate the first gate and a second portion of the second source/drain region proximate the first gate;

forming first and second halo regions of a first dosage beneath the first gate by implanting off-axis through the first opening at a first twist angle and then a second and substantially opposite twist angle, the first mask and the first gate shadowing opposite portions of the substrate lateral to the first gate so that the first halo region forms beneath the first gate proximate the first portion of the first source/drain region and the second halo region forms beneath the first gate proximate the second portion of the second source/drain region;

removing the first mask;

forming a second mask on the substrate, the second mask having a second opening exposing a first portion of the first source region proximate the second gate; and

forming a third halo region of a second dosage greater than the first dosage proximate the first portion of the first source region by implanting off-axis through the second opening, the second mask and the second gate shadowing portions of the substrate lateral to the second gate so that the first halo region forms beneath the first gate proximate the first portion of the first source region, but no halo region is formed proximate the first drain region.

10. The method of claim 9, wherein the second dosage is about twice the first dosage.

11. The method of claim 9, comprising forming the symmetric and asymmetric transistors on a shared active region.

12. The method of claim 9, wherein the symmetric transistor is formed adjacent to the asymmetric transistor.

13. The method of claim 9, wherein the symmetric transistor is not formed adjacent to the asymmetric transistor.

14. The method of claim 9, wherein the first and second halo regions are formed by implanting at a RIGHT twist angle and again at a LEFT twist angle relative to the first gate.

15. The method of claim 14, wherein the third halo region is formed by implanting at a RIGHT twist angle or a LEFT twist angle relative to the second gate.

16. The method of claim 9, wherein the second opening extends to either side of the second gate.

17. The method of claim 16, wherein the second opening extends different distances from opposite sides of the second gate.

18. A method of manufacturing, comprising:

forming a symmetric transistor having a first gate on the substrate, a first source/drain region and second source/drain region in a substrate, a first asymmetric transistor having a second gate on the substrate, a first source region and a first drain region in the substrate, and a second asymmetric transistor having a third gate on the substrate, a second source region adjacent to the first source region and a second drain region;

forming a first mask on the substrate, the first mask having a first opening exposing a first portion of the first source/drain region proximate the first gate and a second portion of the second source/drain region proximate the first gate;

forming first and second halo regions of a first dosage beneath the first gate by implanting off-axis through the first opening at a twist angle and then a second and substantially opposite twist angle, the first mask and the first gate shadowing opposite portions of the substrate lateral to the first gate so that the first halo region forms beneath the first gate proximate the first portion of the first source/drain region and the second halo region forms beneath the first gate proximate the second portion of the second source/drain region;

removing the first mask;

forming a second mask on the substrate, the second mask having a second opening exposing a first portion of the first source region proximate the second gate; and

forming a third halo region of a second dosage greater than the first dosage proximate the first portion of the first source region by implanting off-axis at a third twist angle through the second opening, the second mask and the second gate shadowing portions of the substrate lateral to the second gate so that the first halo region forms beneath the first gate proximate the first portion of the first source region, but no halo region is formed proximate the first drain region;

removing the second mask;

forming a third mask on the substrate, the third mask having a third opening exposing a first portion of the second source region proximate the third gate; and

forming a fourth halo region of a third dosage greater than the first dosage proximate the first portion of the second source region by implanting off-axis at a fourth twist angle substantially opposite to the third twist angle through the second opening, the third mask and the third gate shadowing portions of the substrate lateral to the third gate so that the fourth halo region forms beneath the third gate proximate the first portion of the second source region, but no halo regions are formed proximate the first and second drain regions.

19. The method of claim 18, wherein the second dosage is about twice the first dosage.

20. The method of claim 18, comprising forming the symmetric and the first and second asymmetric transistors on a shared active region.

21. The method of claim 18, wherein the symmetric transistor is formed adjacent to one of the first and second asymmetric transistors.

22. The method of claim 18, wherein the symmetric transistor is not formed adjacent to either of the first and second asymmetric transistors.

23. The method of claim 18, wherein the first and second halo regions are formed by implanting at a RIGHT twist angle and again at a LEFT twist angle relative to the first gate.

24. The method of claim 23, wherein the third halo region is formed by implanting at a RIGHT twist angle or a LEFT twist angle relative to the second gate.

25. The method of claim 24, wherein the fourth halo region is formed by implanting at a RIGHT twist angle or a LEFT twist angle relative to the third gate.

26. The method of claim 18, wherein the second opening extends to either side of the second gate.

27. The method of claim 26, wherein the third opening extends to either side of the third gate.

28. The method of claim 27, wherein the second opening extends different distances from opposite sides of the second gate and the third opening extends different distances from opposite sides of the third gate.